Maharashtra State Board of Technical Education, Mumbai
TEACHING PLAN (TP-TH)/ Course Information Sheet (CIS)

K-1

Academic Year: 2026-27 **Date: 01**/07/2026
Institute Name: K. K. Wagh Polytechnic, Nashik **MSBTE Code:** 0078
Program and Code: Computer Technology (CM) **Course Code &. Abbr.:** 313303 (DTE)
Course Name: Digital Techniques (DTE) **Name of Faculty:** Mr. M.N.Jadhav
Class: SYCM-Lin **Semester:** 3rd **Scheme:** K **Course Index:** CI303 **Learning Hrs:** 45

• Teaching-Learning & Assessment Scheme:

Course Title	Course Code / Abbr	Course Category	Learning Scheme					Credits	TH Paper Duration (Hrs.)	Assessment Scheme											
			Actual Contact Hrs/Week			SLH	NLH			Theory				Based on LL & TSL Practical				Based on SL			Total Marks
			CL	TL	LL					FA TH	SA TH	Total		FA-PR		SA-PR		SLA			
										Max	Max	Max	Min	Max	Min	Max	Min	Max	Min		
Digital Techniques	313303/ DTE	DSC	3	--	2	1	6	3	3	30	70	100	40	25	10	25#	10	25	10		175

Abbreviations: CL- Class Room Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS – Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination, @$ Internal Online Examination

• Course Outcomes (COs) & Theory Learning Outcomes (TLOs):

By learning the course Digital Techniques (DTE -313303) Second year Computer Technology students will be able to :

CO No.	TLO's No.	Course Outcomes (COs) / Theory Learning Outcomes (TLO's)
CO303.1 (CO1)		**Apply number system and codes concept to interpret working of digital systems.**
	TLO 1.1	Convert the given number from onenumber system to another number system.
	TLO 1.2	Perform arithmetic operations onbinary numbers.
	TLO 1.3	Subtract givenbinary numbers using 1's and 2's compliment method.
	TLO 1.4	Convert the given coded number into the other specifiedcode.
	TLO 1.5	Write the application of the givencode.
	TLO 1.6	Perform BCD addition and subtractionfor the given Decimal numbers.
CO303.2 (CO2)		**Apply Boolean laws to minimize complex Boolean function**
	TLO 2.1	Define the given characteristics parameters of the digitallogic families.
	TLO 2.2	Draw symbol and truth table of givenlogic gates.
	TLO 2.3	Explain the concept of Buffer andTristate logic .
	TLO 2.4	Implement basic gates and other gates with the help ofuniversal gate.
	TLO 2.5	Simplify the given expression usingBoolean laws and develop logic circuits
CO303.3 (CO3)		**Develop combinational logic circuits for given applications**
	TLO 3.1	Develop logiccircuits for standard SOP/POS form of the given logic expression.TLO
	TLO 3.2	Minimize the given logic expression using K-map (up to 4 variables).
	TLO 3.3	Design Adder and subtractor using K-map.
	TLO 3.4	Describe working of specified Encoder and Decoder with help of block diagram and truth table.
	TLO 3.5	Describe the working of Multiplexerand Demultiplexer.
CO303.4 (CO4)		**Develop sequential logic circuits using Flip-flops.**
	TLO 4.1	Differentiate between Latch and FlipFlop.
	TLO 4.2	Explain basicmemory cell and use relevant triggering technique for the givendigital circuit.
	TLO 4.3	Describe the truth tables for the givenFlip flops, applications of Flip flops.
	TLO 4.4	Use the giventype of flip flop and itsexcitation table to design specific type counter.

	TLO 4.5	Describe theworking of specified shift register with the help of timing diagram.
	TLO 4.6	Design specified modulo-N counter using Flip flops
	TLO 4.7	Design Ring /Twisted ring counter using given Flip-Flop.
CO303.5 (CO5)		**Interpret functions of data converters and memories in digital electronic systems.**
	TLO 5.1	Describe theworking of the given type of DAC..
	TLO 5.2	Calculate theoutput voltage for the given digital input for specified DAC.
	TLO 5.3	Describe theworking of the given type of ADC.
	TLO 5.4	Compareworking of ROM,EPROM, EEPROM and FlashMemory

Teaching Plan:

Unit No. (Allotted Hrs. & Marks)	COs & TLOs	Unit Title with Topic Details/Contents	Plan Dates (From-To & No. of Lectures)	Actual Execution (From-To & No. of Lectures)	Teaching Method/ Media	Remark
01 (05) 08 Marks	CO1 TLO 1.1	**Unit - I Number Systems** 1.1 Number Systems: Types of Number Systems (Binary, Octal, Decimal, Hexadecimal)	01/07/2026 (01)		Chalk-Board, LCD+PPTs, eNotes, Ref. Book	
	1.2	1.2 Binary Arithmetic: Addition, Subtraction, Multiplication and Division	06/07/2026 (01)		Chalk-Board, LCD+PPTs	
	1.3	1.3 Subtraction using 1's and 2's complement method	08/07/2026 (01)		Chalk-Board, Ref. Book	
	1.4 1.5	1.4 Codes: BCD, Gray code, Excess-3 and ASCII code, Code conversions, Applications of codes. 1.5 BCD Arithmetic: BCD Addition, Subtraction using 9's and 10's complement	13/07/2026 To 15/07/2026 (02)		Chalk-Board, LCD+PPTs, eNotes, MKCL ERA, YouTube Videos	
02 (08) 12 Marks	CO2 TLO 2.1	**Unit - II Logic Gates and Boolean Algebra** 2.1 Logic Families: Characteristics of logic Families- Noise margin, Power dissipation, Figure of merit ,Fan in, Fan out, Speed of operation, maximum clock frequency supply voltage requirement ,power per gate , Comparison of TTL, CMOS and ECL logic family	20/07/2026 To 22/07/2026 (03)		Chalk-Board, LCD+PPTs, eNotes, YouTube Videos	
	2.2 2.4	2.2 Introduction to positive and negative logic systems, Logic Gates: Symbol, Truth table of Basic logic gates as AND, OR,NOT gates ,Universal gates as NAND,NOR and Special purpose gates(EX-OR,EX-NOR).	27/07/2026 To 28/07/2026 (02)		Chalk-Board, LCD+PPTs, eNotes, MKCL ERA, YouTube Videos	
	2.3	2.3 Study Buffer and Tristate logic.	29/07/2026 (01)		Chalk-Board, eNotes,	
	2.5	2.4 Study of laws of Boolean algebra, DualityTheorem ,De-Morgan's theorem with conversions	03/08/2026 To 04/08/2026 (02)		Chalk-Board, LCD+PPTs, eNotes, MKCL ERA, YouTube Videos	

03 (12) 18 Marks	CO3 TLO 3.1	**Unit-III Combinational Logic Circuit** 3.1 Standard Boolean expression: Sum of products [SOP] and Products of Sum [POS], Min-term and Max-term, SOP-POS form conversion, realization using NAND/NOR gates.	05/08/2026 To 18/08/2026 (03)		Chalk-Board, LCD+PPTs, eNotes, YouTube Videos	
	3.2	3.2 Boolean Expression reduction using K-map: Minimization of Boolean expressions (up to 4 variables) using SOP and POS form.	18/08/2026 To 24/08/2026 (03)		Chalk-Board, LCD+PPTs	
	3.3	3.3 Arithmetic circuits : design Half and Full Adder using K- maps, design Half and Full Subtractor using K-maps	25/08/2026 To 25/08/2026 (02)		Chalk-Board, LCD+PPTs, MKCL ERA, YouTube Videos	
	3.4	3.4 Encoder and Decoder: Functions of Encoder and Decoder, Block Diagram and Truth table, Priority Encoder ,BCD to 7 segment Decoder	26/08/2026 To 31/08/2026 (02)		Chalk-Board, LCD+PPTs, eNotes	
04 (12) 18 Marks	3.5	3.5 Multiplexer and Demultiplexer: Working, Truth table and applications of MUX and DEMUX. MUX tree, DEMUX tree, DEMUX as Decoder	01/09/2026 To 01/09/2026 (02)		Chalk-Board, LCD+PPTs, MKCL ERA,	
	CO4 TLO 4.1, 4.2	**Unit - IV Sequential Logic Circuits** 4.1.1 Difference between Combinational and Sequential Logic 4.1.2 Flips- Flops and Latch Introduction 4.1.3 Basic memory cell concept 4.1.4 RS-Latch using NAND and NOR 4.1.5 Triggering methods- Edge & Level	02/09/2026 To 09/09/2026 (05)		Chalk, Blackboard, LCD Projector, PPT	
	4.3	4.2.1 Flip-Flops: S-R, J-K, T and D, Truth table and logic circuits of each flip-flop, 4.2.2 Excitation table, applications of F/F	15/09/2026 To 15/09/2026 (02)		Chalk-Board, LCD+PPTs	
	4.4	4.3 Race around condition in JK flip-flop, Master- Slave JK Flip Flop	16/09/2026 (01)		Chalk-Board, LCD+PPTs	
	4.5	4.4.1 Shift registers- Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out ,Parallel In Parallel Out 4.4.2 Bi-directional Shift register, 4-bit Universal Shift register	21/09/2026 To 22/09/2026 (02)		Chalk-Board, LCD+PPTs	
	4.5, 4.6, 4.7	4.5.1 Counters- Synchronous and Asynchronous counters, Modulus of counter concept 4.5.2 Ripple counter, Ring Counter, Twisted Ring Counter, Up – down counter, Decade Counter, MOD-N counter, Timing Diagram	22/09/2026 To 23/09/2026 (02)		Chalk-Board, LCD+PPTs k-Board, LCD+PPTs, MKCL ERA, YouTube Videos	
05 (08) 14 Marks	CO5 TLO 5.1, 5.2	**Unit - V Data Converters and Memories** 5.1.1 Digital to Analog Data Converter specifications 5.1.2 Circuit diagram and working of R-2R Ladder DAC 5.1.3 Circuit diagram and working of Weighted resistor DAC	28/09/2026 To 29/09/2026 (03)		Chalk-Board, LCD+PPTs k-Board, LCD+PPTs, YouTube Videos	
	5.3	5.2.1 Analog to Digital Data Converter (ADC) : Block Diagram, Types and Working of Dual Slope ADC 5.2.2 Successive Approximation, Flash Type ADC, ADC selection specifications	30/09/2026 To 05/10/2026 (02)		Chalk-Board, LCD+PPTs k-Board, LCD+PPTs,	

	5.4	5.3.1 Memories: Types- Primary memory , Secondary Memory, Memory Bank 5.3.2 Features ,RAM (SRAM, DRAM), Volatile and Non- Volatile, ROM (PROM, EPROM, EEPROM), Flash Memory 5.3.3 Comparison of RAM and ROM,EPROM and Flash Memory, SIMM: Features, SSD memory: Features	06/10/2026 To 07/10/2026 (03)		Chalk-Board, LCD+PPTs k-Board, LCD+PPTs, MKCL ERA, YouTube Videos	

- ## Chapter wise CO-PO Mapping:

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes PSOs	
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PSO-1	PSO-2
CO1	2	--	1	--	--	--	3	1	-
CO2	2	--	2	--	--	--	2	1	1
CO3	3	2	3	2	--	1	2	2	2
CO4	3	2	3	2	--	1	2	2	2
CO5	2	--	2	2	1	1	2	-	2

- **Legends:-** High:03, Medium:02, Low:01, -- :No Mapping

Sr.No.	Programme Outcomes (POs)	Programme Specific Outcomes (PSOs)
1.	**PO-1** Basic and Discipline Specific Knowledge	**PSO1** Apply acquired skills of programming, networking, hardware & database for computer based problem solving and software development. **PSO-2** Pursue higher studies in the field of Computer Science / Computer Engineering /Information Technology.
2.	**PO-2** Problem Analysis	
3.	**PO-3** Design/ Development of Solution	
4.	**PO-4** Engineering Tools	
5.	**PO-5** Engineering Practices for Society, Sustainability and Environment	
6.	**PO-6** Project Management	
7.	**PO-7** Life Long Learning	

- ## Weightage to Learning Efforts & Assessment Purpose (Specification Table)

Sr.No	Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	I	Number Systems	CO1	5	2	4	2	8
2	II	Logic Gates and BooleanAlgebra	CO2	8	2	4	6	12
3	III	Combinational Logic Circuits	CO3	12	4	6	8	18
4	IV	Sequential Logic Circuits	CO4	12	4	6	8	18
5	V	Data Converters and Memories	CO5	8	4	6	4	14
Grand Total				**45**	**16**	**26**	**28**	**70**

*# **Learning Levels with reference to Bloom's Taxonomy:** R Level: Remember, U Level: Understand, A-Level: Apply*

- ## Formative & Summative Assessment Criteria:
  - ### Theory Assessment:

a) Formative assessment (TH-FA) :

- Two offline class tests each of 30 marks will be conducted as per MSBTE guidelines. The average of two class test marks will be consider for final TH-FA(Average) out of 30 marks.

b) Summative Assessment (TH- SA) :

- The comprehensive End semester assessment will be done by MSBTE by a Theory written Examination for 70 marks. Question Paper and Assessment is performed by MSBTE.
- Final Theory Score out of 100 Marks will be derived as the total score as below:
  TH-SA [out of 70] + TH- FA [Average out of 30] = 100 Marks

▪ Practical Assessment:

1. Formative Assessment (FA) of each practical/experiment will be performed progressively for 50 marks. The assessment will be performed based on the Regularity in Practical Performance, Tool Selection Ability, Use of Appropriate tool to perform the Identified tasks, Algorithm/Solution developed, Quality of output achieved, Answer to sample questions and Submit report in total time.
2. Final Term Work (FA-PR) of 25 marks is calculated based on scores in Formative Assessment for all practical's/experiments as:
   Term Work Marks = (Sum of Total Marks Scored in FA / Total Number of Experiments)*25
3. Self-learning Activities (SLA) includes Micro project / Assignment / other activities related to subject/course and it will be evaluated out of 25 Marks.
4. A Summative (comprehensive) Assessment (SA-PR) of Practical will be performed as End Semester Examination (ESE). The SA-PR will be for 25 Marks with MSBTE guidelines at the end of semester. The schedule of MSBTE Practical ESE will be display on Notice board prior to examination.

● References :

1. Suggested Books for Reference:

Sr. No.	Title of Book	Author	Publication
1	Jain R.P	Modern Digital Electronics	McGraw-Hill Publishing, New Delhi,2009 ISBN:9780070669116
2	Anand Kumar	Fundamentals of Digital Circuits	PHI learning Private limited, ISBN:978-81-203-5268-1
3	Salivahanan S, Arivazhagan S.	Digital Circuits and Design	Vikas Publishing House, New Delhi,2013ISBN: 9789325960411
4	Puri.V.K	Digital Electronics	McGraw-Hill Publishing, New Delhi,2016 ISBN:97800746331751
5	Malvino A.P Donald .P. Leach	Digital Principles	McGraw-Hill Education, New DelhiISBN:9789339203405
6	Anil.K.Maini	Digital Electronics: Principles, Devices and Applications	Wiley India, Delhi, 2007, ISBN:9780470032145
7	Floyd, Thomas	Digital Fundamentals	Pearson Education India, Delhi 2014,ISBN:9780132737968
8	G.K.Kharate	Digital Electronics	Publisher: Oxford University Press, ISBN:9780198061830

2. Software Learning Websites:

Sr. No.	Link / Portal	Description
1	https://studytronics.weebly.com/digital-electronics.html	Basics of Digital Electronics
2	https://www.udemy.com/course/basics-of-digital-techniques/	Introduction To Digital Number System & Logic Gates
3	https://www.geeksforgeeks.org/synchronous-sequential-circuit s-in-digital-logic/	Boolean Algebra and Logic Gates, Combinational and Sequential Logic Circuits
4	https://onlinecourses.nptel.ac.in/noc19_ee51/preview	Digital Circuits
5	https://de-iitr.vlabs.ac.in/	Virtual Labs for Digital Systems
6	https://www.tutorialspoint.com/digital_circuits/digital_circ uits_sequential_circuits.htm	Sequential Circuits

3. URLs of Referred Videos:

Sr. No.	Link / Portal	Description
1	https://youtu.be/0lwhoQ5aQe8?si=bY2vqIHmhr4R2_jp	Logic Gates Introduction
2	https://youtu.be/QIyugGzih4k?si=dcauWHRmoN7x_ImN	Binary Code Conversion System
3	https://youtu.be/LTtuYeSmJ2g?si=pF81TD8G7QuCTmHf	Latch & Flip Flop
4	https://youtu.be/fLN1YOmuAr8?si=t_Iu8fr0EvFtnhdf	Sequential Circuits
5	https://youtu.be/NjMX4hohyRI?si=DTAAtybNP2LCCnff	Shift Register

4. Self-Prepared Videos:

Sr. No.	Link / Portal	Description
1	https://youtu.be/mHSF4Yx2jz8?si=S2l3LvtNv5cD7Lgp	Introduction to Logic Gates in Digital Circuit's
2	https://youtu.be/r0EUOYL_D8A?si=88ks-sIP8aCAWgqS	Boolean Expressions & De Morgan's Theorem

1. **Tools :**
   - Google Classroom used for Uploading Learning Material of Course, Assignments, Practice Test etc.
   - MKCL LMS Era – Describe the use of the Tool in Leaning and Assessment

Mr. M.N.Jadhav **(Faculty Name & signature)**

Mr. A.D.Talole **CIAAN Co-ordinator**

Prof. M.P.Bhosale **(HOD-Computer Tech. Dept.)**

CC-

1. DTE – 313303 Course File
2. Notice Board / ERP
3. Institute Website / CIAAN Coordinator